STIC Search Report
EIC 2100

STIC Database Tracking Number: 147161

TO: Jeff Swearingen **Location: Rnd 4C61** **Art Unit : 2145** **Tuesday, March 08, 2005** **Case Serial Number: 09/848443**	**From: David Holloway** **Location: EIC 2100** **RND 4B19** **Phone: 2-3528** **david.holloway@uspto.gov**

Search Notes

Dear Examiner Swearingen,

Attached please find your search results for above-referenced case.
Please contact me if you have any questions or would like a re-focused search.

David

STIC EIC 2100 Search Request Form

147161

Today's Date: 3/8/05

What date would you like to use to limit the search?

Priority Date: 5/3/01 Other:

Name JEFF SWEARINGEN

AU 2145 Examiner # 82494

Room # 4C61 Phone 2-3921

Serial # 09/848,443

Format for Search Results (Circle One):

(PAPER) DISK EMAIL

Where have you searched so far?

(USP) DWPI EPO JPO (ACM) IBM TDB

IEEE INSPEC SPI Other _____

Is this a "Fast & Focused" Search Request? (Circle One) (YES) NO

A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

TAKE A SYNCHRONOUS REQUEST, PROCESS IT ASYNCHRONOUSLY

STIC Searcher Fred Holloway Phone 3-3529

Date picked up 3-8-05 Date Completed 3-8-05

Search and Information Resources Administration

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Set     Items   Description
S1    1199396   SYNCHRONOUS? OR SIMULTANEOUS? OR CONCURRENT? OR SEQUENTIAL-
            LY
S2    1256765   ASYNCHRONOUS OR "NOT"()(SIMULTANEOUS OR CONCURRENT? OR SEQ-
            UENTIAL?) OR PARALLEL?
S3    2948553   TABLE? OR GRID? ? OR NAMESPACE? OR ARRAY? OR MATRIX? OR MA-
            TRICES OR HASH
S4    9776764   MATCH? OR COMPAR? OR LOOKUP OR LOOK()UP OR FIND? OR LOCATE
S5   10336886   SELECT? OR CHOOSE? OR EITHER? OR DETERMIN? OR SELECT? OR P-
            ICK? ?
S6      90217   S1 AND S2
S7      18425   S5 AND S6
S8        675   S3 AND S4 AND S7
S9      54612   S3(2N)S4
S10        51   S8 AND S9
S11     32754   S1(10N)S2
S12      6024   S5 AND S11
S13       344   S12 AND (CONVERT? OR CONVERSION? OR TRANSLAT?)
S14         0   S9 AND S13
S15         1   SYNCHRONOUS()REQUEST AND ASYNCHRONOUS(N)(PROCESS?)
S16        52   S10 OR S15
S17        41   RD (unique items)
S18        33   S17 NOT PY>2001
File   8:Ei Compendex(R) 1970-2005/Jan W3
         (c) 2005 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2005/Feb
         (c) 2005 ProQuest Info&Learning
File  65:Inside Conferences 1993-2005/Mar W1
         (c) 2005 BLDSC all rts. reserv.
File   2:INSPEC 1969-2005/Feb W4
         (c) 2005 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2005/Jan W4
         (c)2005 Japan Science and Tech Corp(JST)
File 111:TGG Natl.Newspaper Index(SM) 1979-2005/Mar 07
         (c) 2005 The Gale Group
File   6:NTIS 1964-2005/Feb W4
         (c) 2005 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2005/Feb W4
         (c) 2005 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2005/Feb W4
         (c) 2005 Inst for Sci Info
File  62:SPIN(R) 1975-2005/Nov W4
         (c) 2005 American Institute of Physics
File  99:Wilson Appl. Sci & Tech Abs 1983-2005/Jan
         (c) 2005 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2005/Jan W5
         (c) 2005 FIZ TECHNIK
```

18/5/12 (Item 12 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01032375 E.I. Monthly No: EI8107055320 E.I. Yearly No: EI81019025
Title: ERROR-CONTROLLING DEVICE FOR HF CHANNELS.
Author: Matic, S. M.; Jankovic, D. J. I.
Corporate Source: Inst Boris Kidric, Belgrade, Yugosl
Source: EUROMICRO Journal (European Association for Microprocessing and Microprogramming) v 6 n 6 Nov 1980 p 395-398
Publication Year: 1980
CODEN: EUJOD4
Language: ENGLISH
Journal Announcement: 8107
Abstract: Practical biprocessor error-controlling equipment (ECE) realized by the INTEL 8085 microprocessors has been demonstrated. Several shorter BCH codes for correction of 1 to 3 errors (codeword length is less or equal to 15) are chosen. The **look - up table** method for encoding and decoding is used. The ECE is intended for use on simplex, half and full duplex channels for the transmission rates of 50-9600 b/s; both forward error correction and hybrid techniques are implemented. Variable modes of operation such as **synchronous** and **asynchronous** transmission with variable stop bit length, different character lengths with or without parity control, different transmission rates can be **selected** by the switches on the front panel. 7 refs.
Descriptors: *COMPUTERS, MICROPROCESSOR; CODES, SYMBOLIC
Classification Codes:
722 (Computer Hardware); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

18/5/13 (Item 13 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00834266 E.I. Monthly No: EI7907050066 E.I. Yearly No: EI79015543
Title: COMPARISON **OF** SELECTED ARRAY **PROCESSOR ARCHITECTURES.**
Author: Hufnagel, Stephen P.
Corporate Source: Univ of Tex, Austin
Source: Computer Design v 18 n 3 Mar 1979 p 151-158
Publication Year: 1979
CODEN: CMPDAM ISSN: 0010-4566
Language: ENGLISH
Journal Announcement: 7907
Abstract: Examination of **synchronous parallel** pipelined and **asynchronous parallel array** processor architectures points out differing hardware/software concepts, memory utilization, input/output flexibility, and processing capabilities. 7 refs.
Descriptors: *COMPUTER ARCHITECTURE
Identifiers: **ARRAY** PROCESSOR
Classification Codes:
722 (Computer Hardware); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

15/5/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02074049 JICST ACCESSION NUMBER: 94A0450226 FILE SEGMENT: JICST-E
X-window programming.3.Client and X server.
ENDO TOMOHIRO (1)
(1) Somu
BIT(Tokyo), 1994, VOL.26,NO.6, PAGE.48-57, TBL.1
JOURNAL NUMBER: G0873AAS ISSN NO: 0385-6984
UNIVERSAL DECIMAL CLASSIFICATION: 681.3.066
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: X lib has various functions offered by X server which clients can conveniently utilize, because Xlib is a library in position of the binding of C language of X protocol. As a character of the functions of Xlib, the following are explained; 1) Design of a non- **synchronous request** , 2) buffering of a request, 3) batch processing of a request, 4) cash memory of data structure. The connection of network communication based on X protocol between client and X server is described.
DESCRIPTORS: window system; UNIX; protocol; interprocess communication; computer programming; **asynchronous processing** ; batch processing; link connecting; distributed processing; client server system
BROADER DESCRIPTORS: method; operating system; system program; computer program; software; rule; computer processing system; treatment; link operating; communication operation; operation(processing); connection; computer system(hardware); system
CLASSIFICATION CODE(S): JD03020J

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Set      Items   Description
S1      789609   SYNCHRONOUS? OR SIMULTANEOUS? OR CONCURRENT? OR SEQUENTIAL-
             LY
S2      922519   ASYNCHRONOUS OR "NOT"()(SIMULTANEOUS OR CONCURRENT? OR SEQ-
             UENTIAL?) OR PARALLEL?
S3      883050   TABLE? OR GRID? ? OR NAMESPACE? OR ARRAY? OR MATRIX? OR MA-
             TRICES OR HASH
S4     1442806   MATCH? OR COMPAR? OR LOOKUP OR LOOK()UP OR FIND? OR LOCATE
S5     2848472   SELECT? OR CHOOSE? OR EITHER? OR DETERMIN? OR SELECT? OR P-
             ICK? ?
S6       56603   S1 AND S2
S7       12266   S5 AND S6
S8         335   S3 AND S4 AND S7
S9       15153   S3(2N)S4
S10         48   S8 AND S9
S11      13741   S1(10N)S2
S12       3103   S5 AND S11
S13        568   S12 AND (CONVERT? OR CONVERSION? OR TRANSLAT?)
S14         35   S13 AND IC=G06F-015?
S15         15   S10 AND IC=G06F?
S16         49   S14 OR S15
S17         46   S16 NOT AD>20010503
File 347:JAPIO Nov 1976-2004/Oct(Updated 050209)
         (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200515
         (c) 2005  Thomson Derwent
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17/5/14 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016634727 **Image available**
WPI Acc No: 2004-793440/200478
Related WPI Acc No: 2000-137482; 2000-171171; 2000-171184; 2000-223672; 2000-223674; 2000-572419; 2000-572420; 2000-594484; 2001-080393; 2001-159204; 2001-182565; 2001-374135; 2001-397249; 2001-397398; 2001-397455; 2001-441396; 2001-451474; 2001-521889; 2002-195105; 2002-414303; 2002-434254; 2002-470963; 2002-739473; 2003-554312; 2003-749674; 2003-831552; 2003-900098; 2004-279863; 2004-279864; 2004-398201; 2004-650711; 2004-661037; 2004-675071; 2004-687651; 2005-109963
XRPX Acc No: N04-625159

Method for searching address table **in network switch, involves dividing** lookup table **into two sub-** tables **, and** comparing **desired entry to stored entries within one sub-** table **until one of the stored entries is equal to desired entry**

Patent Assignee: BROADCOM CORP (BROA-N)
Inventor: JORDA M A; KALAPATHY P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6810037	B1	20041026	US 99124878	P	19990317	200478	B
			US 99135603	P	19990524		
			US 99149706	P	19990820		
			US 2000528164	A	20000317		

Priority Applications (No Type Date): US 2000528164 A 20000317; US 99124878 P 19990317; US 99135603 P 19990524; US 99149706 P 19990820
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6810037	B1		84	H04L-012/28	Provisional application US 99124878
					Provisional application US 99135603
					Provisional application US 99149706

Abstract (Basic): US 6810037 B1

NOVELTY - A primary **lookup table** is divided into two sub- **tables** , and a desired entry is **compared** with the stored entries within one of the sub- **table** until one of the stored entries is equal to the desired entry. If a hit is not **determined** for the desired entry, the desired entry is **compared** with the stored entries within another sub- **table** .

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for network switch.

USE - For searching primary address **table** in network switch (claimed) of local area communication network such as token ring, **asynchronous** transfer mode (ATM) network, Ethernet, fast Ethernet and gigabit Ethernet environments.

ADVANTAGE - By splitting the **lookup table** into sub- **tables** , it is possible to search for two separate packet addresses **simultaneously** in **parallel** , thereby nearly doubling throughput even through the actual time required to complete each individual **lookup** does not change. Thus increases the performance of the address **lookup** time over a single **table** , without requiring the use of additional memory.

DESCRIPTION OF DRAWING(S) - The figure shows a general block diagram of the network switch.

Ethernet port interface controllers (20)
gigabit port interface controller (30)
internet port interface controller (90)
common buffer pool (50)
memory management unit (70)
pp; 84 DwgNo 1/47

Title Terms: METHOD; SEARCH; ADDRESS; **TABLE** ; NETWORK; SWITCH; DIVIDE; **TABLE** ; TWO; SUB; **TABLE** ; **COMPARE** ; ENTER; STORAGE; ENTER; ONE; SUB; **TABLE** ; ONE; STORAGE; ENTER; EQUAL; ENTER
Derwent Class: T01; W01

International Patent Class (Main): H04L-012/28
International Patent Class (Additional): **G06F-015/167**
File Segment: EPI

17/5/15 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011372687 **Image available**
WPI Acc No: 1997-350594/199732
XRPX Acc No: N97-290659

Data input apparatus for D-A converter **in automatic alignment monitor test system - has serial-to-parallel interface which receives data access request from auto-alignment adaptor and uses logic decoder to** select **D-A** converter **input according to mode to be tested**

Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: LEE M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5644757	A	19970701	US 95489385	A	19950612	199732	B

Priority Applications (No Type Date): US 95489385 A 19950612
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5644757	A		8		

Abstract (Basic): US 5644757 A

The apparatus includes a serial-to-parallel interface which receives a data access request issued by an auto-alignment device. The serial-to-parallel interface includes a device for **converting** a number of sequential data bits into parallel form for **conversion** by a D/A **converter** into analog. A logic decoder **selects** one of a number of D/A **converter** output channels to output the **converted** analog signal to a monitor. A set of buffers is connected between the serial-to-parallel interface of a microcontroller and the auto-alignment device.

The set of buffers is also connected to the CPU of the microcontroller and relays signals issued by the CPU to the serial-to-parallel interface. A convening device includes a digital logic device which receives an enabling signal to initiate **conversion** of the sequential data bits into **parallel** form. Each of the data bits is **sequentially** shifted into a multi-bit register at a rising edge of one corresponding clock signal pulse supplied to the digital logic device.

USE/ADVANTAGE - E.g. video monitor display testing under specific display mode. CPU not required to implement D/A **converter** access, reducing overall hardware and firmware complexity and cost. Efficient data accessing.

Dwg.1/6

Title Terms: DATA; INPUT; APPARATUS; DIGITAL-ANALOGUE; **CONVERTER** ; AUTOMATIC; ALIGN; MONITOR; TEST; SYSTEM; SERIAL; PARALLEL; INTERFACE; RECEIVE; DATA; ACCESS; REQUEST; AUTO; ALIGN; ADAPT; LOGIC; DECODE; **SELECT** ; DIGITAL-ANALOGUE; **CONVERTER** ; INPUT; ACCORD; MODE; TEST
Derwent Class: T01; T04; W02
International Patent Class (Main): **G06F-015/00**
International Patent Class (Additional): H04N-017/00
File Segment: EPI

17/5/17 **(Item 4 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

011113696 **Image available**
WPI Acc No: 1997-091621/199709
XRPX Acc No: N97-075529

Parallel- conversion compiler parallel processing program forming method for distributed memory type parallel computer system - involves inserting code which performs distributed conversion , when shape of distributed type of data of input-output processing differs in memory and external memory

Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8328871	A	19961213	JP 95133082	A	19950531	199709	B

Priority Applications (No Type Date): JP 95133082 A 19950531
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8328871	A		27	G06F-009/45	

Abstract (Basic): JP 8328871 A

The method involves sequential searching of the input-output sentence of a processing program. A code which **determines** whether a file that is the objective of the input-output sentence processing is the objective for parallel input-outputs, or it is the objective for sequential input-outputs, is inserted.

A **parallel** input-output processing or input-output processing is **sequentially** performed between some memories and some external memories according to a decision result. When the shape of distributed type of data of the input-output processing differs on the memory and the external memory, the code which performs a distributed **conversion** is inserted.

ADVANTAGE - **Converts** sequential processing program with input-output sentence, to program for distributed memory type parallel computer with parallel input-output function. Prevents redn. of **conversion** ability. Improves speed by forming parallel processing program. Alters file which objective of input-output processing during execution of parallel processing program. Performs parallel input-output processing of data other than array data.

Dwg.2/24

Title Terms: PARALLEL; **CONVERT** ; COMPILE; PARALLEL; PROCESS; PROGRAM; FORMING; METHOD; DISTRIBUTE; MEMORY; TYPE; PARALLEL; COMPUTER; SYSTEM; INSERT; CODE; PERFORMANCE; DISTRIBUTE; **CONVERT** ; SHAPE; DISTRIBUTE; TYPE ; DATA; INPUT; OUTPUT; PROCESS; DIFFER; MEMORY; EXTERNAL; MEMORY
Derwent Class: T01
International Patent Class (Main): G06F-009/45
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

17/5/21 **(Item 8 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

010375459 **Image available**
WPI Acc No: 1995-276773/199537
XRPX Acc No: N95-211671

Interface mechanism for generating asynchronous processing operations in parallel processing environments - receives procedure call from first processing operation and invoke data object function for second processing operation

Patent Assignee: ARJOMANDI E (ARJO-I); IBM CANADA LTD (IBMC); INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: ARJOMANDI E; OFARRELL W G; O'FARRELL W G
Number of Countries: 006 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 667575	A2	19950816	EP 95300699	A	19950203	199537	B
CA 2115464	A	19950812	CA 2115464	A	19940211	199544	
JP 8110860	A	19960430	JP 9517582	A	19950206	199627	
CA 2115464	C	19981215	CA 2115464	A	19940211	199909	
US 5999987	A	19991207	US 95385628	A	19950209	200004	
EP 667575	B1	20010926	EP 95300699	A	19950203	200157	
DE 69522842	E	20011031	DE 622842	A	19950203	200173	
			EP 95300699	A	19950203		

Priority Applications (No Type Date): CA 2115464 A 19940211
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 667575	A2	E	14	G06F-009/46	
Designated States (Regional): DE FR GB					
CA 2115464	A			G06F-015/16	
JP 8110860	A		14	G06F-009/44	
CA 2115464	C			G06F-015/16	
US 5999987	A			G06F-009/46	
EP 667575	B1	E		G06F-009/46	
Designated States (Regional): DE FR GB					
DE 69522842	E			G06F-009/46	Based on patent EP 667575

Abstract (Basic): EP 667575 A

The interface mechanism includes a pointer which **converts** a procedure call into an asynchronous task thread, while returning an expected response to permit a calling program to continue processing. The returned value is **either** discarded or **converted** to a future variable if the calling program requires the result of the separate processing on the asynchronous thread.

The mechanism includes a first linker for receiving a procedure call from a first processing operation in association with one of the memory facilities and for issuing a response to resume the first processing operation. A register is provided for invoking a data object function for a second processing operation in association with another of the memory facilities alongside the first processing operation.

USE/ADVANTAGE - **Concurrent** processing in object, oriented **parallel** multiprocessor environments. Permits multiple **asynchronous** processing operations without compiler modifications, language extensions or pre-processing in object-oriented languages e.g. C ++.

Dwg.1/3

Title Terms: INTERFACE; MECHANISM; GENERATE; ASYNCHRONOUS; PROCESS; OPERATE ; PARALLEL; PROCESS; ENVIRONMENT; RECEIVE; PROCEDURE; CALL; FIRST; PROCESS; OPERATE; INVOKE; DATA; OBJECT; FUNCTION; SECOND; PROCESS; OPERATE
Derwent Class: T01
International Patent Class (Main): G06F-009/44; G06F-009/46; **G06F-015/16**
International Patent Class (Additional): G06F-009/45
File Segment: EPI

17/5/31 **(Item 18 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

008822922 **Image available**
WPI Acc No: 1991-326935/199145
Related WPI Acc No: 1991-326934; 1991-333984; 1991-353954; 1991-353955; 1992-416275; 1995-311233; 1995-320246; 1998-062605
XRPX Acc No: N91-250441

Scalable compound instruction set machine architecture - statically analyses sequence of instructions prior to instruction decode to determine which are executed in parallel

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: BLANER B; VASSILIADIS S; VASSILIADI S; JEREMIAH T L
Number of Countries: 015 Number of Patents: 011
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 454985	A	19911106	EP 91104323	A	19910320	199145	B
HU 57455	T	19911128				199151	
CA 2039640	A	19911105				199205	
CS 9100936	A	19911217				199209	
EP 454985	A3	19940330	EP 91104323	A	19910320	199521	
US 5502826	A	19960326	US 90519384	A	19900504	199618	
			US 9313982	A	19930205		
			US 94186221	A	19940125		
EP 454985	B1	19961218	EP 91104323	A	19910320	199704	
DE 69123629	E	19970130	DE 623629	A	19910320	199710	
			EP 91104323	A	19910320		
US 5732234	A	19980324	US 90519384	A	19900504	199819	
			US 9313982	A	19930205		
			US 94186221	A	19940125		
			US 95452773	A	19950530		
			US 96699689	A	19960815		
CA 2039640	C	20000111	CA 2039640	A	19910403	200023	
EP 545927	B1	20000628	EP 91908085	A	19910329	200035	
			WO 91US2037	A	19910329		
			EP 97119948	A	19910329		

Priority Applications (No Type Date): US 90519384 A 19900504; US 9313982 A 19930205; US 94186221 A 19940125; US 95452773 A 19950530; US 96699689 A 19960815; US 90519382 A 19900504; US 90543458 A 19900626; US 91642011 A 19910115
Cited Patents: NoSR.Pub; 3.Jnl.Ref; EP 449661; EP 52194; JP 61245239; US 4295193; US 4574348; US 4586127; US 4594655; US 4755966; US 4760520; US 4780820; US 4807115; US 4847755; US 4942525
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 454985	A		36		
Designated States (Regional): AT CH DE ES FR GB IT LI NL SE					
US 5502826	A		30	G06F-009/44	Cont of application US 90519384
					Cont of application US 9313982
EP 454985	B1	E	38	G06F-009/38	
Designated States (Regional): AT CH DE DK ES FR GB IT LI NL SE					
DE 69123629	E			G06F-009/38	Based on patent EP 454985
US 5732234	A		29	G06F-009/30	Div ex application US 90519384
					Cont of application US 9313982
					Cont of application US 94186221
					Cont of application US 95452773
					Cont of patent US 5502826
CA 2039640	C	E		G06F-009/38	
EP 545927	B1	E		G06F-009/30	Related to application EP 97119948
					Related to patent EP 825529
					Based on patent WO 9117496
Designated States (Regional): AT CH DE FR GB IT LI NL SE					

Abstract (Basic): EP 454985 A
The machine provides processing which looks for classes of instructions that can be executed in **parallel** without data dependent

or hardware-dependent interlocks. Certain of the existing instructions are allocated into multiple categories which are **compared** with the categories of adjacent existing instructions in an instruction stream to detremine whether the adjacent existing instructions are capable of **parallel** execution in the particular configuration of a data processing system.

Those capable of **parallel** execution are identified with a compounding indicator. The result is a stream of scalar instructions compounded or grouped together before instruction decode so that they are already flagged and identified for **selective simultaneous parallel** execution by execution units.

USE/ADVANTAGE - For **parallel** processing by computer. Minimises interlocks (pipeline hazards). (36pp Dwg.No.1/17)

Title Terms: COMPOUND; INSTRUCTION; SET; MACHINE; ARCHITECTURE; STATIC; ANALYSE; SEQUENCE; INSTRUCTION; PRIOR; INSTRUCTION; DECODE; **DETERMINE** ; EXECUTE; **PARALLEL**

Derwent Class: T01

International Patent Class (Main): **G06F-009/30** ; **G06F-009/38** ; **G06F-009/44**

International Patent Class (Additional): **G06F-012/00** ; **G06F-015/80**

File Segment: EPI

17/5/41 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004830424
WPI Acc No: 1986-333765/198651
XRPX Acc No: N86-248904

Data management appts. for automatic flight system - has two independent processors and data stores with separate data paths to avoid error transfer between processors

Patent Assignee: HONEYWELL INC (HONE); SPERRY CORP (SPER)
Inventor: DAVIDSON D D; ENDRUD D G; DAVIDSON S S
Number of Countries: 010 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 205274	A	19861217	EP 86303985	A	19860527	198651	B
BR 8601026	A	19870113				198708	
US 4713757	A	19871215	US 85743535	A	19850611	198806	
ES 8800453	A	19880101	ES 555898	A	19860610	198809	
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DE 3687765	G	19930325	DE 3687765	A	19860527	199313	
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Priority Applications (No Type Date): US 85743535 A 19850611
Cited Patents: 1.Jnl.Ref; A3...8912; EP 44218; FR 2484668; No-SR.Pub; US 4156932; US 4217486
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 205274	A	E	9		
	Designated States (Regional): DE FR GB IT NL				
EP 205274	B1	E	12	G06F-015/50	
	Designated States (Regional): DE FR GB IT NL				
DE 3687765	G			G06F-015/50	Based on patent EP 205274

Abstract (Basic): EP 205274 B

Data signals input to the apparatus from sources such as sensor sub-systems of an aircraft are **converted** from bit serial format to parallel format and supplied to a parallel data bus. Data acquisition is controlled by a first processor whilst a second processor functions independently to perform its normal routines. Data received are stored by the first processor in its associated data store.

The data received are supplied **simultaneously** and independently from the serial- **parallel converter** to an independent data store over a data path which is independent of the first processor. The second processor acts to control transfer of data stored in the independent store to its associated second data store.

ADVANTAGE - Errors introduced into data after transmission will be detected by at least one of processors and an error in one processor is not transferred to other processor over data paths. (9pp Dwg.No.0/7

Title Terms: DATA; MANAGEMENT; APPARATUS; AUTOMATIC; FLIGHT; SYSTEM; TWO; INDEPENDENT; PROCESSOR; DATA; STORAGE; SEPARATE; DATA; PATH; AVOID; ERROR ; TRANSFER; PROCESSOR
Derwent Class: T01
International Patent Class (Main): **G06F-015/50**
International Patent Class (Additional): G05D-001/00; G06F-011/16; **G06F-015/16**
File Segment: EPI

17/5/46 **(Item 33 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

003073661
WPI Acc No: 1981-H3700D/198132
Differential equations solving system - uses second group of resolvers, two adders and divider coupled to controls for iteration self-tuning during solving
Patent Assignee: TAGANROG WIRELESS ENG (TAWI)
Inventor: FRADKIN B G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
SU 771674	B	19801015				198132 B

Priority Applications (No Type Date): SU 2631467 A 19780619
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SU 771674	B		7		

Abstract (Basic): SU 771674 B

Partial derivatives differential equations computing unit use resolvers, adders and divider to increase computing speed. Two groups of resolvers are connected to computer via **converter** and to buffer memory. First group of resolvers incorporate data input, registers, multiphase and adders. Second group of resolvers contain data inputs adders and multiplier.

Computer data is applied in **parallel** to buffer memory from which it is sensed **sequentially** by digits and **parallel** by words. Data format is **converted** before applying to resolvers. First group resolvers compute iterations vectors, second **determine** optimal iteration parameters.

Iteration results are multiplied divided and added to boundary condition data from buffer memory. Total results are formed in an adder. Iteration cycle is repeated until 'stop' signal is received from controls. Introduction of additional resolver adders and divider allow **determination** of iterations optimal convergence. Bul.38/ 15.10.80. (7pp)

Title Terms: DIFFERENTIAL; EQUATE; SOLVING; SYSTEM; SECOND; GROUP; RESOLUTION; TWO; ADDER; DIVIDE; COUPLE; CONTROL; ITERATIVE; SELF; TUNE; SOLVING
Derwent Class: T01
International Patent Class (Additional): **G06F-015/32**
File Segment: EPI